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Design of a Sample and Hold Circuit using Rail to Rail Low Voltage Compact Operational Amplifier and bootstrap Switching

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Abstract:
This paper presents a low power high performance and higher sampling speed sample and hold circuit. The proposed circuit is designed at 180 nm technology and has high linearity. The circuit can be used for the ADC frontend applications and supports double sampling architecture. The proposed sample and hold circuit has common mode range beyond rail to rail and uses two differential pairs transistor stages connected in parallel as its input stage.
Keywords: Differential Operation Amplifier, Rail to Rail Input, Sample and Hold, Constant Transconductance

I. Introduction

In this paper a switched capacitor sample and hold circuit has been proposed. The circuit operates at a supply voltage of 1.2 volts and has a sampling frequency of 80 MS/s. The main blocks of a sample and hold circuit are amplifier, sampling capacitor and switches. Gain and slew rate of the amplifier determine the resolution and sampling speed of the circuit. The switches are responsible for the charge injection which degrades the accuracy. Here we have worked on the amplifier to increase bit accuracy of the circuit. Along with that we have used bootstrapped switch to avoid signal dependent charge injection. The paper is divided into sections which briefly describe the amplifier input stage, the architecture of amplifier, bootstrap switch and at the end simulation results are presented.

II. Amplifier Design

The amplifier being used here has a rail to rail common mode input stage which is described below. The other stages include summing circuit then class AB control and at the end output transistors. At input stage complementary differential pairs are connected in parallel to get a rail to rail input range. This technique assures that at least one differential input stage will work from the two applied stages. The rail to rail input technique is shown in fig1. When the both pairs of input differential stage operate then the net transconductance is given by:

$$g_{mT} = g_{mn} + g_{mp}$$

Since the individual differential-pair transconductances gm, and g_m, are well-defined functions of the of the tail currents I, and I_p, respectively, common mode current biasing is required to implement this scheme.

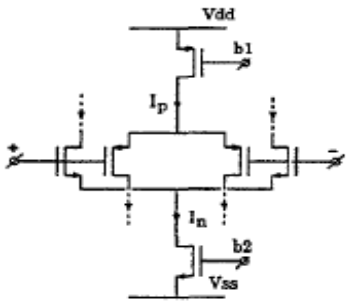

Fig.1. Complementary differential pair

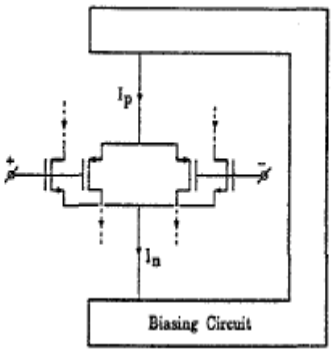

Fig.2. Schematic of Rail to Rail input stage with common mode biasing

In other words, we balance the reduction in g_m,(g_m,) (caused by the reduction of I_n (I_p) when V_{inCM} approaches V_{ss}(V_{dd}) by increasing I_P (I_n) to make transconductance independent of common mode level. The scheme is shown in fig.2 [2].

Compact Two-Stage Op-amp

The compact two stage operational amplifier requires a minimum supply voltage equal to its gate-source

voltage and two saturation voltages which is of the order 1.2-1.5V [3]. The motive of this paper is to develop an amplifier topology that combines operation to a supply voltage equal to gate-source voltage and two saturation voltages using a compact two stage structure offering high power efficiency and small die area. A low voltage two stage op-amp is shown below:

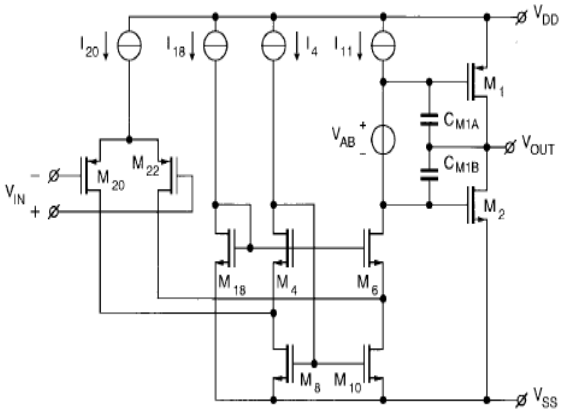

Fig.3. Compact Low Voltage Op-amp

The basic topology of a low-voltage compact op-amp is shown in Fig.3. The amplifier consists of a P-channel (P) MOS input stage M_{20}, M22 a current mirror M_8, M_{10} cascades M_4, M_6 and a rail-to-rail output stage M_1, M_2. A PMOS input stage is used to allow common-mode voltages down to and below the negative supply rail. The current mirror is needed to sum the opposite-phase signals of the differential input stage in order to drive the gates of the rail-to-rail output stage in phase. The cascodes provide the necessary level shift between input and output stage. Further, M_6 provides gain by leaving the high input impedance of the gates of the output stage intact. The rail-to-rail output stage allows rail to-rail output-signal swing, making efficient use of the supply voltage. By biasing the output stage in class AB, the supply current is used efficiently. The class-AB biasing is in principle represented by the voltage source, V_{AB} which expresses all its important properties. To set the quiescent current, the sum of the gate-source voltages of the output stage can be controlled in such a way that it is equal to the sum of a reference PMOS gate-source voltage $V_{GS,P}$ and an N-channel (N)MOS gate source voltage V_{GSN} , which is obtained by giving V_{AB} the value:

$$\mathbf{V_{AB}= V_{DD}-V_{SS}-V_{GSp} - V_{GSn}} \qquad (1)$$

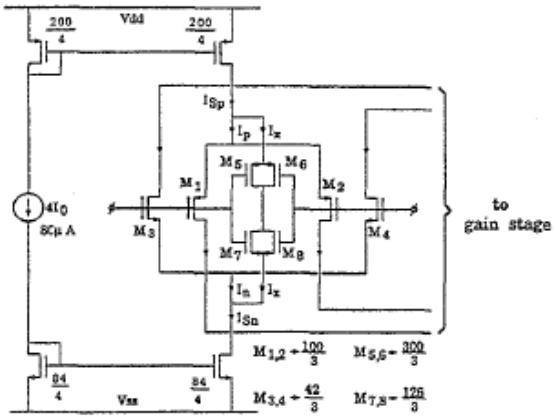

Fig. 4(a). Proposed Constant g_m rail to rail input stage

The circuit for the rail to rail input stage is shown in fig.2 (a) which is used as an input stage for the proposed low voltage compact architecture shown in fig.4 (b).

The input stage, shown in Fig. 4(a) replaces the conventional input stage in the proposed architecture. The aspect ratios of the four additional transistors in the Fig. 4(a) circuit are three times that of the corresponding differential-pair transistors. The nominal value of the tail currents I_{sn} and I_{sp} is $4I_o$ and must be selected sufficiently large to ensure strong-inversion operation.

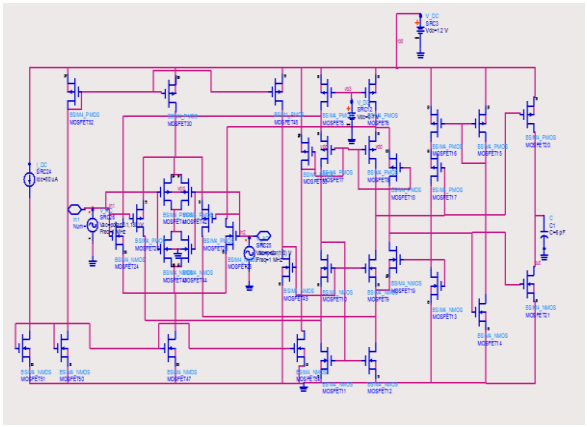

Fig.4 (b). Low Voltage Compact Op amp architecture with folded mesh and constant g_m rail to rail input stage

The currents I_x and $I_P= Is_p-I_x(Is_n-I_x)$ conducted by the two differential pair transistors are given as:

1). V_{inCM} close to Vss: $I_x= 3/4I_{sn}=o$
2). $I_n=1/4I_{sn}=0$
3). $I_p=I_{sp}-I_x= 4I_o-I_x=4I_0$

1). V_{inCM} near mid supply: $I_x= 3I_o$
2). $I_n= Is_n-I_x =4I_o-3I_0= I_o$
3). $I_p=I_{sp}-I_x= 4I_o-3I_0= I_o$

1). V_{inCM} close to V_{dd}: I_x= 3/4I_{sp}=o
2). I_n= Is_n-I_x=4I_0
3). I_p=I/4$_{sp}$=0

The rail-to-rail input stage has a g_m-control circuit. Therefore, the simple summing circuit of the first op-amp can be used. The rail-to-rail input stage consists of PMOS input pair and NMOS input pair. In this input stage the bias current requirement is less and total g_m is less dependent on variation in mobility ratio of NMOS and PMOS which varies by 30% in a fabricated design.

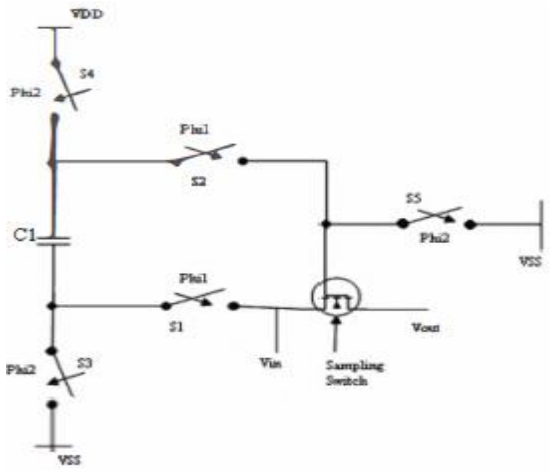

Fig.5. Bootstrap Switch

III. The bootstrap switch

The switch in sample and hold can be implemented using simple NMOS transistor but it has several limitations like input dependent finite ON-resistance and input dependent charge injection. In order to improve the performance of switch NMOS transistor can be replaced by a CMOS switch; proper selection of transistors aspect ratio minimizes the distortion but this is not an effective solution. One of the commonly used techniques to solve the above problems is bootstrap switch [9]. The basic bootstrap switch implementation is shown in **fig 5**. Here capacitor C1 used as a floating battery with a value V_{DD}. Rail to Rail Operational amplifier circuit diagram switch is off through switch s5 and capacitor C1is charged to V_{DD} through switches s3 and s4. In sampling phase this voltage value is applied between gate and source of sampling switch using switches sl and s2. Although the boosted NMOS switch has good distortion characteristics; the required boost voltage is a tradeoff. In addition to the increased circuit complexity the use of the boosted voltage may cause reliability problems and increase the switching noise on the substrate. In the present sample and hold implementation a reliable bootstrap technique is selected which has a maximum voltage of V_{DD} across a single device. This makes design free from oxide reliability issues.

IV. Complete design considerations

As discussed previously the basic blocks of sample and hold circuits are sampling capacitor, op-amp and a switch. The size of the sampling capacitor depends on the KT/C noise. In order to reduce the KT/C noise the sampling capacitor value can be found using [9]

$$C_S > \frac{KT.12}{2^{-2N}.V_{FS}^2} \qquad (2)$$

Where N is the number of bits and VFS is the Full scale ADC voltage, for a 10 bit ADC the required sampling capacitor value to reduce KT/C noise is greater than l.3pF.In this implementation a sampling capacitor of 1. 5pF value is selected.

In order to achieve rail to rail operation and 10 bit accuracy amplifier gain can be calculated using eq (3) [9]

$$A_0 = \frac{2^{N+1}}{\beta} \qquad (3)$$

Where N is number of bits and β is the feedback factor. Using this equation the minimum gain for 13 bit accuracy can be obtained to be 86.26dB. Other important parameters needed for operational amplifier are unity gain frequency and slew rate. The gain bandwidth product (GBW) needed to allow the output voltage to settle with in ±1/2 LSB during the time t_{se} (settling time) is given by:

$$f_t = \frac{1}{2\Pi\beta t_{se}} = \frac{7.6}{2\Pi\beta t_{se}} \qquad (4)$$

and the slew rate of the op-amp can be found using:

$$SR = \frac{k.V_{max}}{T_s} \qquad (5)$$

Simulation Results:

The low voltage compact op-amp architecture with the rail to rail input is shown in the fig.4. has been used to implement the complete design of sample and hold circuit. The implementation has been shown in **fig.7.** The gain and phase plot of the amplifier used are shown below **fig.6**. The gain obtained is 86.823 dB with phase margin of 65.6 degree and f_u=398.3 MHz.

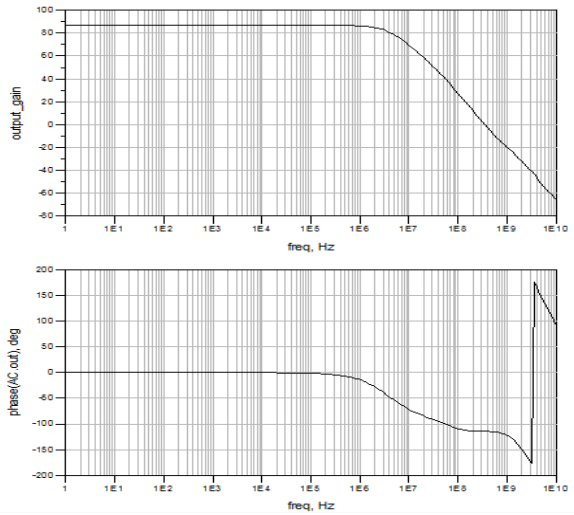

Fig.6. Phase and gain plots of the amplifier

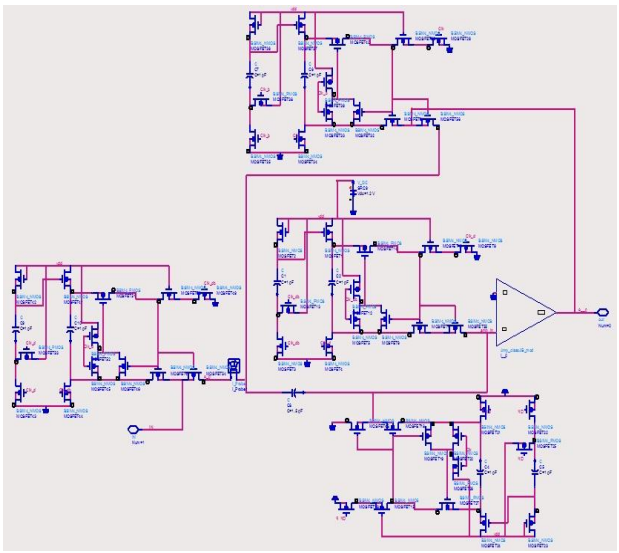

Fig.7. The sample and hold architecture with bootstrap switches

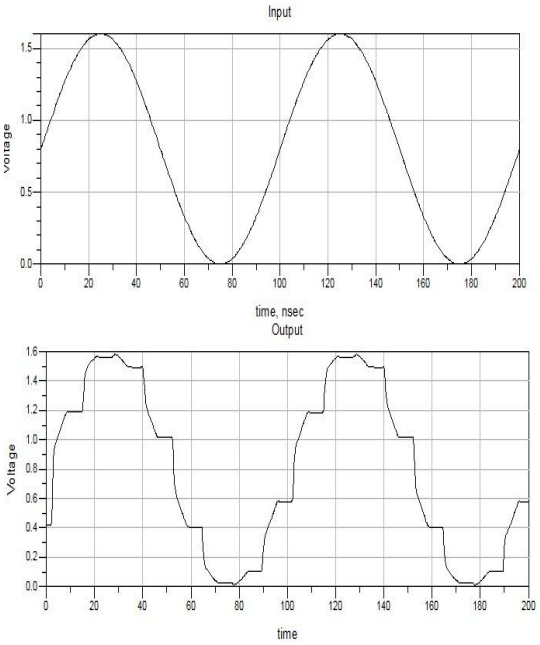

Fig.8. Input and Output waveform of Sample and Hold Circuit

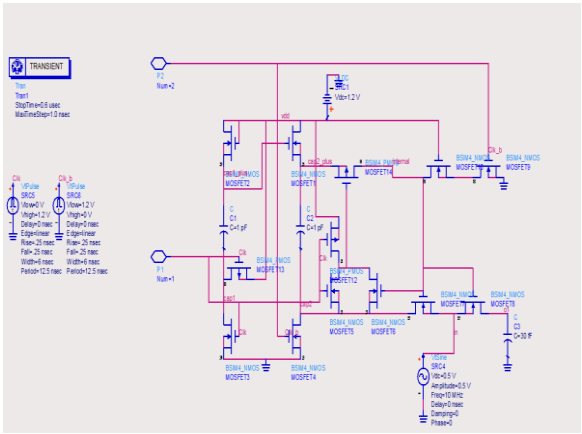

Fig.9. Schematic of bootstrap switch

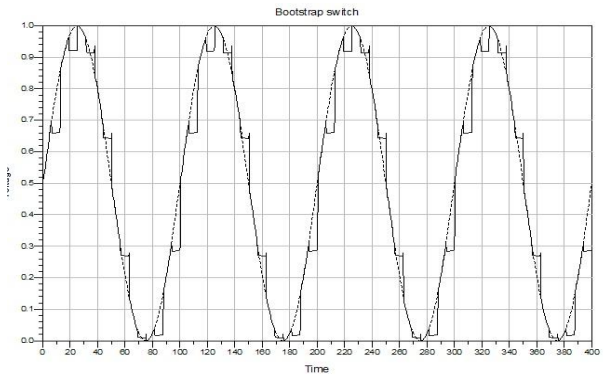

Fig.10. Output Waveforms of Bootstrap Switch

Parameter	Ref 4	Ref 5	Ref 6	Ref 7	Ref 8	This work
Technology (um)	1.2	0.25	0.35	0.5	0.18	0.18
VDD (V)	5 V	1.5	1.5	1.2	1.2	1.2
No. of bits	10	12	NA	NA	10	13
Fs(MS/s)	50	75	50	40	80	80
Power (mW)	47	16	2.6	1.2	4.1	3.89

Table.1. Comparison of current work with previous designs

V. Conclusion

We have designed a sample and hold circuit using rail to rail input stage operational amplifier which is more efficient than the previous designs and bootstrap switches have been used in this circuit. The bit resolution of the architecture is 13 bit with sampling speed of 80MS/sec. The simulation results and comparison results show the enhancement in performance of the sample and hold circuit.

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